What is claimed is:

1. A CMOS image sensor, comprising:

a pixel sensor having a reset mode, the pixel sensor generating reset data in the reset mode, the pixel sensor further generating signal data, the pixel sensor being responsive to energy received externally, for generating the signal data, the pixel sensor producing an amount of photo-charge according to the amount of the received energy and converting the produced photo-charge to the signal data, the signal data having a voltage level depending on the amount of the produced photo-charge;

a data I/O line carrying the signal data and the reset data generated in the pixel sensor;

a double sampling circuit coupled to the data I/O line for sampling the signal data and the reset data, and driving an output terminal; and

an output circuit for outputting data related to a voltage level of the output terminal,

wherein the double sampling circuit samples the signal data before sampling the reset data.

2. The CMOS image sensor in accordance with claim 1, wherein the pixel sensor comprises:

a common junction node;

a reset transistor having a source connected to the common junction node and a drain receiving an externally supplied power voltage, the reset transistor being gated in response to a reset signal;

a photo-diode generating the signal data;

a driving transistor having a gate connected to the common junction node and a drain receiving the external power voltage; and

a selecting transistor transferring a source voltage of the driving transistor to the data I/O line in response to a first selecting signal.

3. The CMOS image sensor in accordance with claim 2, wherein the reset transistor, the driving transistor and the selecting transistor are each N-channel metal oxide semiconductor (NMOS) transistors.

4. The CMOS image sensor in accordance with claim 2, wherein the first selecting signal is a

row-selecting signal for selecting a row of a pixel array.

5. A CMOS image sensor, comprising:

a pixel sensor generating signal data, and generating reset data in a reset mode, the pixel sensor including

a common junction node,

a reset transistor having a source connected to the common junction node and a drain receiving an externally supplied power voltage, the reset transistor being gated in response to a reset signal,

a photo-diode receiving energy externally of the pixel sensor and producing an amount of photo-charge according to the amount of the received energy, the photo-diode converting the produced photo-charge to signal data, the signal data having a voltage level depending on the amount of the produced photo-charge,

a driving transistor having a gate connected to the common junction node and a drain receiving the external power voltage, and

a selecting transistor transferring a source voltage of the driving transistor to the data I/O line in response to a first selecting signal;

a data I/O line carrying the generated signal data and reset data;

a double sampling circuit coupled to the data I/O line for sampling the signal data and the reset data, and driving an output terminal; and

an output circuit for outputting data related to a voltage level of the output terminal,

wherein the double sampling circuit samples the signal data before sampling the reset data.

6. The CMOS image sensor in accordance with claim 5, wherein the reset transistor, the driving transistor and the selecting transistor are each N-channel metal oxide semiconductor (NMOS) transistors.

7. The CMOS image sensor in accordance with claim 5, wherein the first selecting signal is a row-selecting signal for selecting a row of a pixel array.

8. The CMOS image sensor in accordance with claim 1, wherein the double sampling circuit

comprises:

a first transistor driving the data I/O line to a first reference voltage in response to a read command, and outputting a value related to the signal data;

a coupling capacitor coupling a storing node with the data I/O line;

a second transistor driving the storing node to a second reference voltage in response to a control signal; and

a third transistor transferring a voltage of the storing node to the output terminal in response to a second selecting signal.

9. The CMOS image sensor in accordance with claim 8, wherein the first reference voltage is a ground voltage (VSS).

10. The CMOS image sensor in accordance with claim 8, wherein the second reference voltage is a ground voltage (VSS).

11. The CMOS image sensor in accordance with claim 8, wherein the first transistor and the second transistor are each N-channel metal oxide semiconductor (NMOS) transistors.

12. The CMOS image sensor in accordance with claim 8, wherein the second selecting signal is a column-selecting signal for selecting a column of a pixel array.

13. The CMOS image sensor in accordance with claim 8, wherein the coupling capacitor has a terminal connected to the data I/O line.

14. A method for driving an image sensor, including:

(a) providing CMOS image sensor having a plurality of pixel sensors arranged in rows and columns and that generates reset data during a reset mode and generates signal data depending on an amount of photo-charge produced in response to energy received externally, the method comprising the steps of:

(b) generating a read signal and activating a row-selecting signal for selecting one of the rows.

(c) activating a data output signal;

(d) outputting the signal data in response to the data output signal;

(e) driving the reset mode after the step (d); and

(f) outputting the reset data.